DATA SHEET

74AHC2G125; 74AHCT2G125
Bus buffer/line driver; 3-state

Product specification

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Philips
Semiconductors

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Bus buffer/line driver; 3-state 74AHC2G125; 74AHCT2G125

FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- SOT505-2 and SOT765-1 package
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC2G/AHCT2G125 is a high-speed Si-gate CMOS device.

The 74AHC2G/AHCT2G125 provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($n\overline{OE}$). A HIGH at pin $n\overline{OE}$ causes the output to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC2G	AHCT2G	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	3.4	3.4	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	9	11	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC2G125DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	A25
74AHCT2G125DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	C25
74AHC2G125DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	A25
74AHCT2G125DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	C25

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{OE}$	output enable input (active LOW)
2	1A	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	1Y	data output
7	$2\overline{OE}$	output enable input (active LOW)
8	V_{CC}	supply voltage

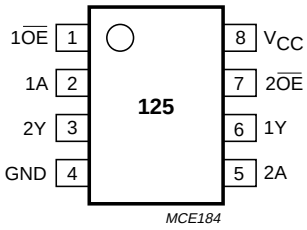


Fig.1 Pin configuration.

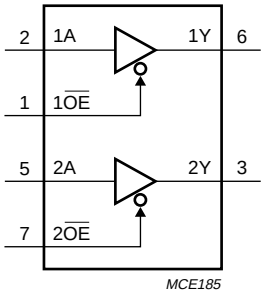


Fig.2 Logic symbol.

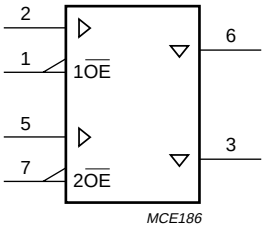


Fig.3 IEC logic symbol.

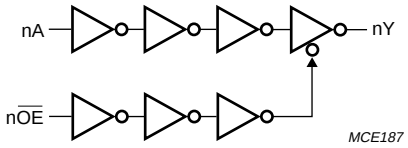


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC2G125			74AHCT2G125			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 ± 0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ± 0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V	–	–20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C	–	250	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Type 74AHC2G125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	2.0	–	V
		I_O = –50 μA	3.0	2.9	3.0	–	V
		I_O = –50 μA	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	3.0	2.58	–	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	2.0	–	0	0.1	V
		I_O = 50 μA	3.0	–	0	0.1	V
		I_O = 50 μA	4.5	–	0	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.36	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	0.25	μA
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	1.0	μA
C_I	input capacitance		–	–	1.5	10	pF

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	–	–	V
		I_O = –50 μA	3.0	2.9	–	–	V
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.48	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	2.0	–	–	0.1	V
		I_O = 50 μA	3.0	–	–	0.1	V
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.44	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	2.5	μA
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	10	μA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	–	–	V
		I_O = –50 μA	3.0	2.9	–	–	V
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.40	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	2.0	–	–	0.1	V
		I_O = 50 μA	3.0	–	–	0.1	V
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.55	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	10	μA
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	2.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
C_I	input capacitance		–	–	–	10	pF

Type 74AHCT2G125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	4.5	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	0	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	0.25	μA
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	1.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0	5.5	–	–	1.35	mA
C_I	input capacitance			–	1.5	10	pF
T_{amb} = –40 to +85 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	2.5	μA
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0	5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{OZ}	3-state output OFF-state current	V_I = V_{CC} or GND	5.5	–	–	10	μA
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	2.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0	5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

AC CHARACTERISTICS

Type 74AHC2G125

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)				
T_{amb} = 25 °C							
V_{CC} = 3.0 to 3.6 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	4.7	8.0	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	–	5.0	8.0	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	–	6.0	9.7	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	6.6	11.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	–	6.9	11.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	–	8.3	13.2	ns
V_{CC} = 4.5 to 5.5 V; note 2							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	3.4	5.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	–	3.6	5.1	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	–	4.1	6.8	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	4.8	7.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	–	4.9	7.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	–	5.7	8.8	ns
T_{amb} = −40 to +85 °C							
V_{CC} = 3.0 to 3.6 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	9.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	9.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	11.5	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	13.0	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	13.0	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	15.0	ns
V_{CC} = 4.5 to 5.5 V; note 2							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)				
T_{amb} = −40 to +125 °C							
V_{CC} = 3.0 to 3.6 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	11.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	11.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	12.5	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	14.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	14.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	16.5	ns
V_{CC} = 4.5 to 5.5 V; note 2							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	7.0	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	6.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	8.5	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	9.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	9.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	11.0	ns

Notes

1. All typical values are measured at V_{CC} = 3.3 V.
2. All typical values are measured at V_{CC} = 5.0 V.

Type 74AHCT2G125

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

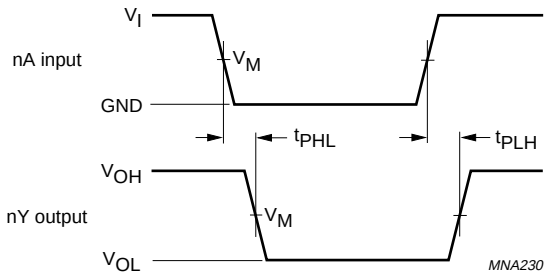
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)				
T_{amb} = 25 °C							
V_{CC} = 4.5 to 5.5 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	–	3.4	5.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	–	3.9	5.1	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	–	4.5	6.8	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	–	4.8	7.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	–	5.1	7.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	50	–	6.1	8.8	ns
T_{amb} = −40 to +85 °C							
V_{CC} = 4.5 to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t_{PZH}/t_{PZL}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t_{PHZ}/t_{PLZ}	propagation delay $n\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)				
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns
T_{amb} = −40 to +125 °C							
V_{CC} = 4.5 to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	15	1.0	–	6.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	6.0	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	15	1.0	–	8.0	ns
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 5 and 7	50	1.0	–	8.5	ns
t_{PZH}/t_{PZL}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	8.5	ns
t_{PHZ}/t_{PLZ}	propagation delay n$\overline{OE}$ to nY	see Figs 6 and 7	50	1.0	–	10.0	ns

Note

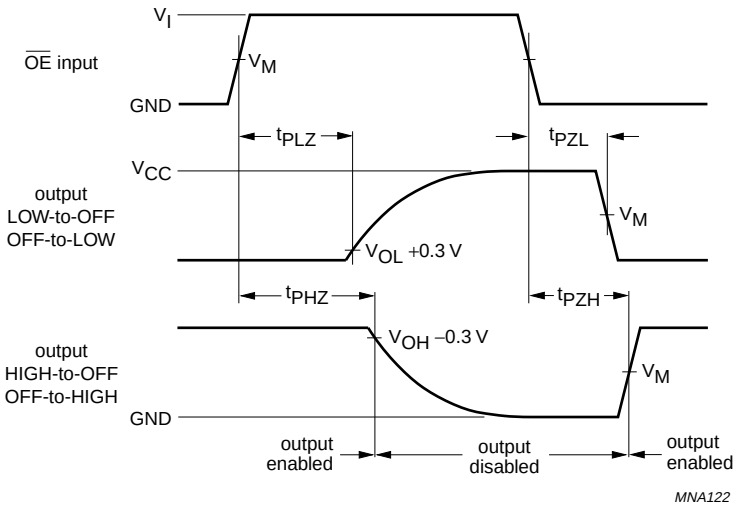
1. All typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS



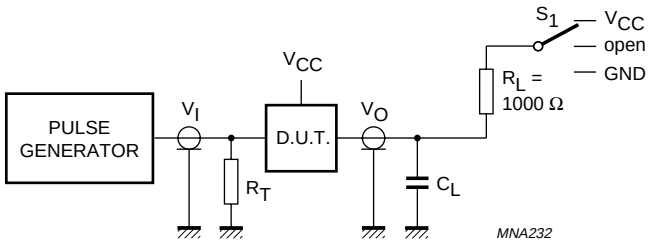
FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC2G125	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT2G125	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.5 The input (nA) to output (nY) propagation delays.



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC2G125	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT2G125	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.6 The 3-state enable and disable times.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

R_L = load resistance.

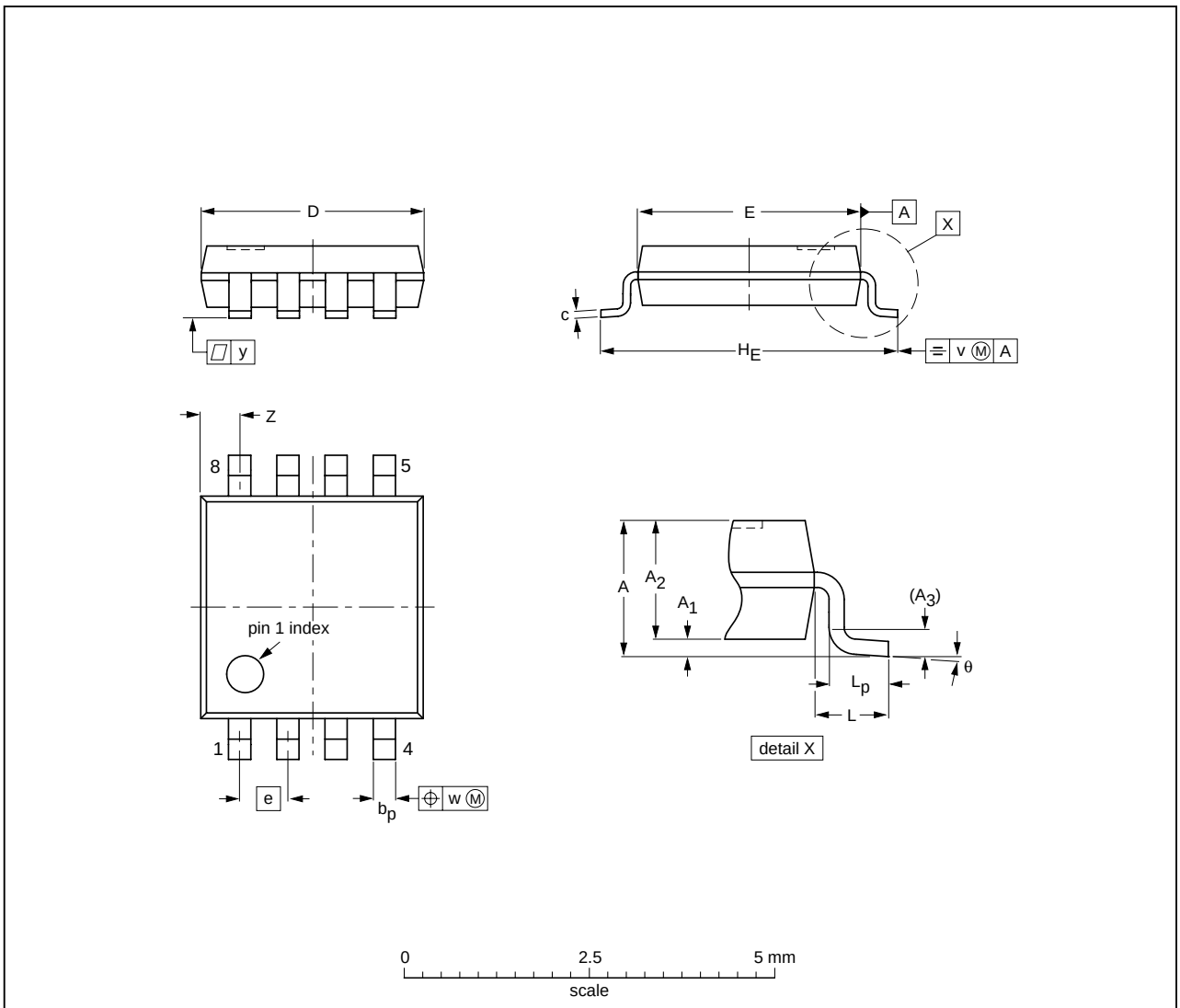
C_L = load capacitance including jig and probe capacitance (see Chapter “AC characteristics” for the value).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

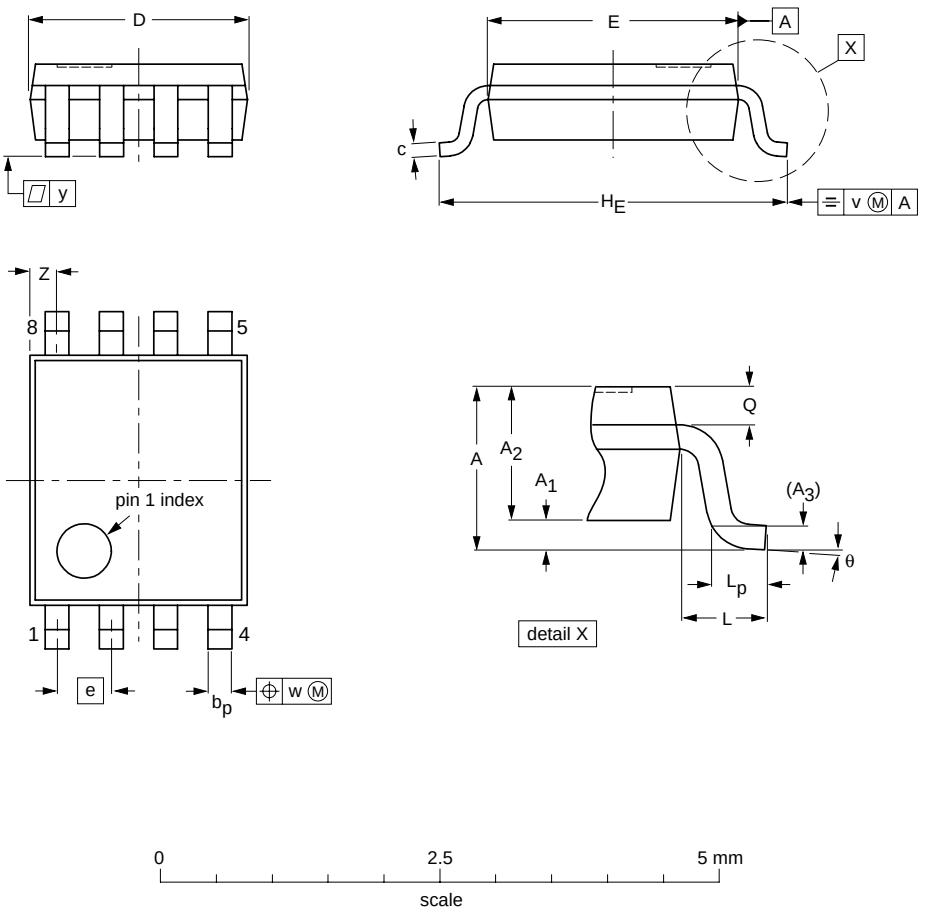
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

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II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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